Lasers in Manufacturing Conference 2017

Fast high yield cutting of 4 and 6 inch SiC-wafer using thermal laser separation (TLS)

Christian Belgardt[a,*], Reinhard Kosuch[a], Dirk Lewke[a], Michael Grimm[a] and Hans-Ulrich Zühlke[a]

[a]3D-Micromac AG, Technologie-Campus 8, 09126 Chemnitz, Germany

Abstract

TLS-Dicing™ is a kerf free laser based separation technology. After development of the basic principle [1] and the demonstration of high separation quality [2] current work is focused on yield improvement. First we investigated the influence of structures inside dicing street on the TLS process. Two different laser wavelengths were used to figure out how to minimize the influence of metal structures, minimization of particles and reduction of heat affected zones on the scribe process. The resulting parameters we applied on thin 4-inch SiC wafers and thick 6-inch SiC wafers. During this work performance indicator values like yield, throughput and chip quality were determined. A very high geometrical yield of more than 96 % could be verified. Finally, observed potential risks of yield loss are discussed and transferred into design rules and best practice based dicing rules.

Keywords: laser dicing; SiC wafer; semiconductor production; kerf free

1. Introduction

Due to certain qualities such as a high band gap, a high saturation velocity, high chemical resistivity, and high thermal conductivity Silicon carbide (SiC) is considered as replacement material for silicon (Si)-based semiconductors like power electronics or sensors for harsh environments [3]. SiC is a crystalline compound of silicon and carbon which is extremely brittle and hard. With 9.2 on the Mohs scale it is almost as hard as diamond which has a hardness of 10 [4]. Currently SiC wafers are mainly mechanically diced with a very low feed rate (4-10 mm/s for standard saw and 10-20 mm/s with ultrasonic support [5]). However in the last two

* Corresponding author. Tel.: +49-371-400-430
E-mail address: belgardt@3d-micromac.com

decades the diameter of the 4H-SiC wafer has increased from 25 to 100 mm and currently the transition to 150 mm diameter is ongoing. Mechanical sawing will reach its limit since the cumulated street length more than doubles and for very small devices it is beyond the ability of one saw blade to completely cut an entire wafer.

TLS-Dicing™ is a novel laser dicing approach for brittle materials such as SiC-based semiconductor products. In the described case study, a typical power device wafer with full backside metallization, polyimide (PI) and metal structures in the dicing streets and a blank wafer of standard thickness were separated by using this technology. Finally the mechanical yield was evaluated.

2. Thermal Laser Separation (TLS)

The TLS technology is based on a two-step process consisting of scribing and cleaving. First a laser scribe initiates a crack along the dicing street and cuts through metal structures at the surface of the wafer. The interaction zone of this scribing process is approximately 10 µm wide and 10 – 15 µm deep. To cleave the already scribed path a thermally induced mechanical stress is used. A continuous wave (cw) laser heats up the solid, brittle material and generates a zone of compressive stress, surrounded by a zone of tangential tensile stress pattern (Fig. 1). The heated zone is followed by a cooling jet of small amount deionized (DI) water that creates a cooled zone with a minimum distance to the heated zone—inducing a tangential tensile stress pattern. The resulting tensile stress in the overlaying region of both stress patterns has a local maximum that is sharply focused and has a clear orientation (perpendicular to the street), and thus is able to open and guide the crack tip through the material. Cleaving with TLS-Dicing™ separates the whole thickness of the wafer with one pass.

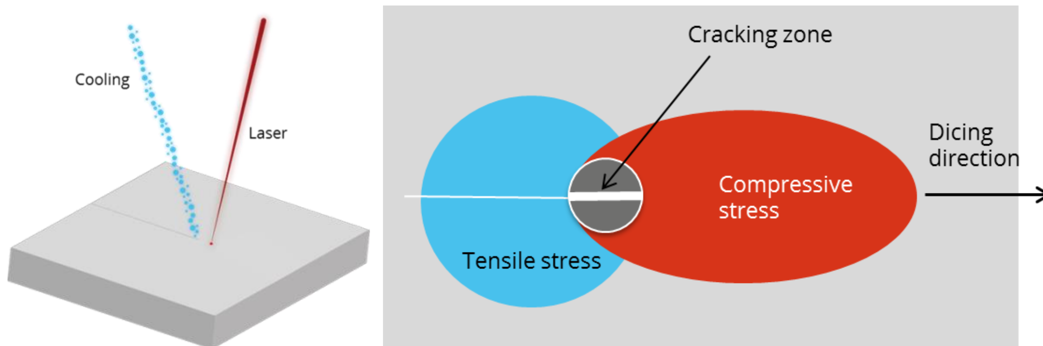

Fig. 1. Principle of TLS

TLS-Dicing™ is a fast, clean and cost-effective alternative to separate SiC-based semiconductor products. Compared to established technologies such as blade sawing and laser ablation the TLS technology has lot of advantages. The high feed rate (>200 mm/s for SiC) enables a high throughput (e.g.: 10 wafers per hour for 4-inch wafer with 2x2 mm² die size). Due to the smooth edges with nearly no chipping and micro cracks the breaking strength is increased and an improvement of electrical properties for vertical devices is provided. With this technology it is possible to separate wafer with thin metal layers on backside without delamination. There are nearly no consumables and no tool wear necessary, this is leading to a low cost of ownership.

Due to the fact that TLS-Dicing™ is a cleaving process, the die edges are smooth and free of remaining stress or micro cracks and chipping zone (Fig. 2). In addition, the backside metal is separated without delamination and heat affects.

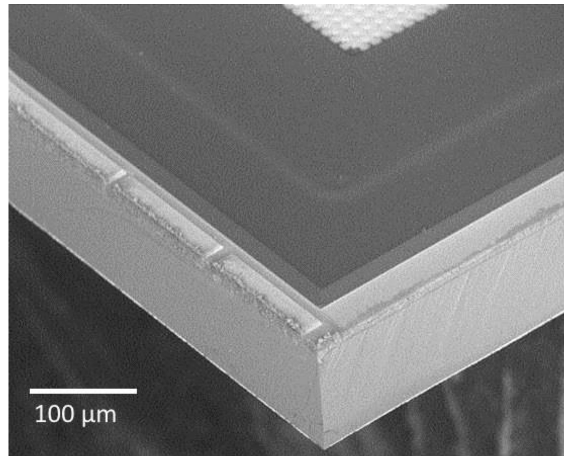

Fig. 2. REM picture of SiC die edge after TLS-Dicing™ process shows smooth edges without micro cracks and chipping.

3. Experimental section

In order to remove the reflecting PCM structures in the streets and to improve straightness of the cleaving line, a continuous scribe along the entire street length was applied. The scribing was done by two different short-pulsed lasers with 532 and 1064 nm wavelength. The scribing speed was variated between 50 and 200 mm/s. To ensure correct focus position at surface a fast z-axis autofocus was used. The cleaving was realized by a 200 W continuous waver (cw) laser with near infrared (NIR) wavelength in combination with a water spray cooling. The consumption of cooling liquid (DI-water) was below 10 ml/min. The wafer wasn't treated with any washing, cleaning or protective coating. To evaluate the mechanical yield of TLS-Dicing™ two experiments were performed with 100 mm and 150 mm SiC wafers. The wafer separation was done by TLS technology with a microDICE® system.

Fig. 3. (a) Diced quarter of 4-inch SiC wafer; (b) 4-inch SiC wafer; (c) mapping of diced 6-inch SiC wafer

4-inch wafers with 110 µm thickness and a thin silver-type backside metal stack was processed (Fig. 3b). The streets were contained several metal test structures for process control monitoring (PCM). The active zone of the dies was passivated by a polyimide (PI) coating. The outer part of the edge exclusion zone was covered by a ring of metallization and PI coating. To simulate a chip size of approx. 4x4 mm², 3x3 clusters of smaller chips were combined and only every third street was diced (Fig. 3a). The determined parameters were also transferred to a blank 6-inch SiC wafer of 350 µm thickness with a thin silver-type backside metal layer (Fig. 3c).

The completely diced wafers were analyzed with a high-resolution optical inspection tool to detect defects and deviations to determine the resulting yield. All dies in the edge exclusion zone have not been included in the consideration.

Additionally 106 dies from a comparable wafer have been packaged into semiconductor housing. After packaging the leakage currents were determined. The packaging and the electrical measurement have been done by the manufacturer of the wafers.

4. Results and discussion

Before cleaving the wafer, a variation of scribing parameters was done. It was found that, independently of the laser wavelength, there are two processing regimes depending on the pulse-to-pulse distance – thermal ablation and single pulse ablation (Fig. 4). On the one hand, a minimal pulse to pulse distance leads to an increase of thermal effects, such as enlargement of heat affected zone (HAZ) and remaining amount of melt. On the other hand with a large pulse-to-pules spacing, higher pulse energy is necessary for a considerable ablation. This creates unwanted micro cracks, generates more particles and increases the influence of PCM structures on the depth of emerging scribe. Another effect could be observed in case of PI in the scribing line. The lower the scribing speed, the smaller the heat affected zone of the PI cover layer. This can be attributed to the resulting plasma plum which interacts with the PI. The final scribing parameters were done with a moderate pulse-to-pulse distance as well as moderate pulse energy with laser wavelength of 532 nm.

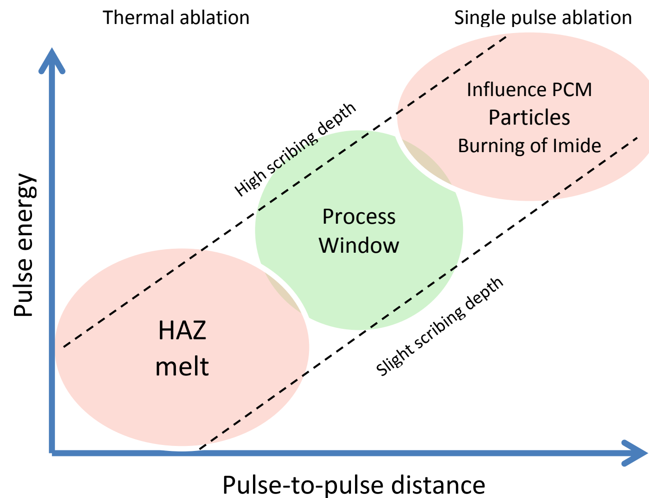

Fig. 4. Schematic for process regimes of scribing parameters.

It could be demonstrated that TLS-Dicing™ leads to a separation without any chipping or micro cracks (Fig. 5a). The backside metal was separated without any delamination (Fig. 5b). This is important in order to perform a proper die attach during assembly. At the edge of the diced chips there is no thermal impact on the PI layer visible.

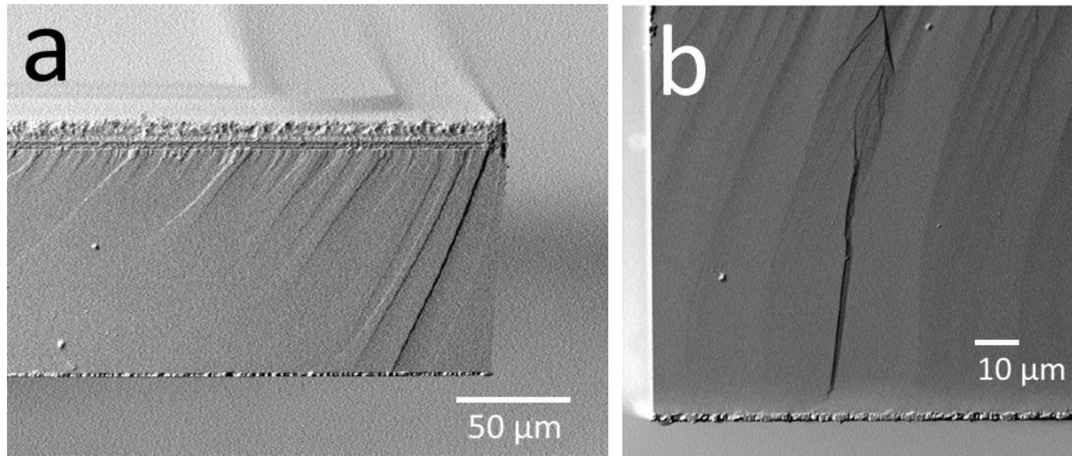

Fig. 5. REM picture, (a) corner of separated die; (b) smooth separation of backside metal

An average value for geometrical yield of 98.9 % (4-inch wafer) [6] and 97.8 % (6-inch wafer) were obtained from evaluation of optical inspection of the diced wafers. All observed deviations and defects have been categorized (Table 1). Almost all of the faults are located in the edge exclusion zone.

Table 1. Resulting average yield and yield losses by categories

Defect Category	Yield [%] 4-inch [6]	Yield [%] 6-inch
Perfect	97,97	94,20
Minor straightness deviation	0,94	2,99
Major straightness deviation	0,23	2,28
Total Yield (all usable dies)	98,91	97,18

A typical fault was a short, local cleave dislocation, nearly perpendicular to the edge of the wafer. This is because of a sudden discharge of local stresses in the wafer due to the metallization layer of the outer rim. In all cases, these deviations were limited to the region of the edge exclusion (Fig. 6a) and can be ignored for yield calculation. Another observed fault was a small deviation of cleaving line without damaging of the active die area (Fig. 6b and Table 1, minor straightness deviation). Also there was no impairment of the yield. In very rare cases the cleaving line touched the active die area (Table 1, major straightness deviation) whereby the two adjoining chips were spoiled with a resulting yield loss. This is mainly related to an overlaying of internal stress pattern.

The electrical measurements of the packaged dies after thermo-cycling revealed that only one out of 106 dies failed the leakage current test. However it is suspected that the cause of this defect is unrelated to the TLS-process.

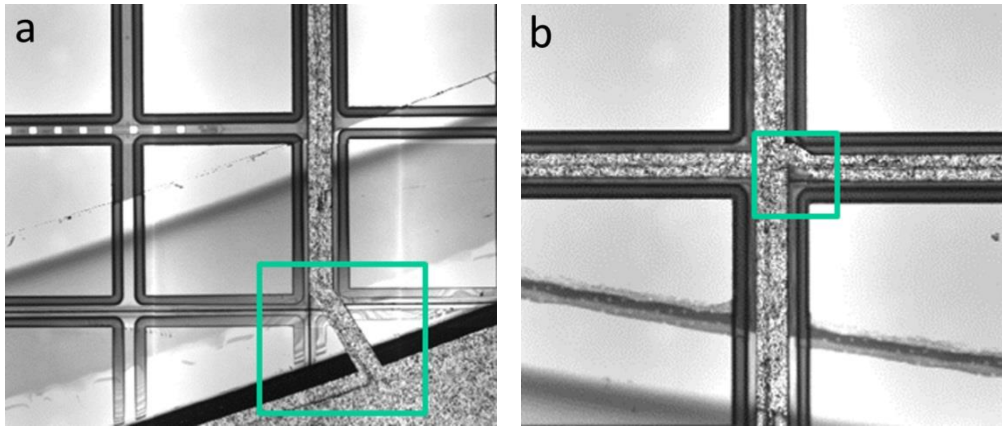

Fig. 6. (a) Example of minor deviation, no influence on the electrical function; (b) Deviation at the wafer's edge, not yield relevant metal

5. Conclusion

As shown TLS-Dicing™ is a new technology to separating SiC. The main benefits are the high throughput, low cost and the high-edge quality of the diced chips. For a standard 100 mm wafer of 110 µm thickness a yield of 98.9 % could be demonstrated. A value of 97.1 % could be achieved for the separation yield of a blank 150 mm Wafer with 350 µm thickness. It is also possible to separate thin backside metal layers and PCM structures in the dicing street.

The diced 100 mm wafer was covered with a metal and PI layer at the outer ring in the edge exclusion area on the top side of the wafer. This ring caused internal stress and dislocations of the cleaving line; same applies to the PCM structures. It is to be expected that with an adaptation of the layout of this areas, an improvement of the total yield would be possible. If a change of the design rules are not possible, another option would be an additional laser step, to remove these obstacles bevor the scribing process.

Acknowledgements

Thanks for partly support of this work to our partners from Fraunhofer IISB located in Erlangen. This work was partly funded by the European Union within the project SEA4KET (Contract number: 611332).

References

[1] Lewke, D., Dohnke K. O., Zühlke, H.-U., Cerezuela Barreto, M., Schellenberger, M., Bauer, A., Ryssel, H., 2015, Thermal Laser Separation – A Novel Dicing Technology Fulfilling the Demands of Volume Manufacturing of 4H-SiC Devices. Materials Science Forum 821-823, P. 528–532

[2] Lewke, D. et al., 2014, High quality and high speed cutting of 4H-SiC JFET wafers including PCM structures by using Thermal Laser Separation, MRS Spring Meeting 2014

[3] Kimoto, T., Cooper, J. A., 2014, Fundamentals of Sillicon Carbide Technology, Growth, Characterization, Devices, and Applications, John Wiley & Sons Singapore PTE Ltd

[4] Mukherjee, S., 2012, Applied Mineralogy: Applications in Industry and Environment, Springer Science & Business Media, pp. 373–

[5] DISCO Technical Review, Mar. 2016

[6] H.-U. Zühlke, M. Gebhardt, 2012, Dicing silicon carbide power devices using thermal laser separation, Chip Scale Review November/December 2016; Volume 20, Number 6